Fraunhofer Institut
Integrierte Schaltungen

Digital Radio Mondiale (DRM)
Base Band Processing IP

Data Sheet, Summary (V1.0)

– subject to change –

Contact

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1 Overview

About DRM. There is a global trend towards the adoption of digital technology in radio and communications, especially for distribution and transmission. Digitalization offers many substantial advantages to national and international broadcasters and infocasters. DRM is the only universal, non-proprietary digital AM radio system with near-FM sound quality available to markets worldwide. Besides providing near-FM quality audio, the DRM system has the capacity to integrate data and text. This additional content can be displayed on DRM receivers to enhance the listening experience. Unlike digital systems that require a new frequency allocation, DRM uses existing AM broadcast frequency bands (below 30 MHz). The DRM signal is designed to fit in within the existing AM broadcast band plan, based on signals of 9 kHz or10 kHz bandwidth.

About the CorePool DRM Solution. Fraunhofer IIS[1] has been contributing for more than 10 years to digital radio, including Eureka DAB, WorldSpace Digital Radio, XM Satellite Radio and has been continuously involved in DRM for about 5 years. Fraunhofer IIS was among the first to provide a real-time DRM receiver reference implementation, the so called "Fraunhofer DRM Software Radio". This implementation of a "DRM radio receiver" runs on a standard PC and uses an external RF front end (e.g. professional shortwave tuner); all digital base band, service and audio decoding is done on the PC in software. The "Fraunhofer DRM Software Radio" was used in all major field tests and is a mature and stable basis to derive DRM receiver products.

The CorePool DRM base band processing IP offers a "pure hardware" solution for Digital Radio Mondiale (DRM) base band decoding. This base band IP may be easily combined with service demultiplexing and audio decoding (AAC/SBR, HVXC, CELP) software libraries running on an embedded ARM9 core or any other host processor. The combination of both IPs, together with an analog tuner front end based on COTS components offers an extremely competitive low cost and low power DRM receiver implementation for the mass market.

The key features of the DRM base band IP are:

- Implements the complete DRM base band processing, including signal acquisition and tracking, signal conditioning, viterbi and multi-level decoding

[1] CorePool is a brand name of Fraunhofer Gesellschaft, represented by Fraunhofer IIS

- Interfaces to standard (analog) tuner frond ends and outputs digital bit stream (DRM service multiplex, MDI) to service/audio decoder
- Fully synthesizeable, independent of any specific semiconductor manufacturer or process
- Free of third-party intellectual property cores (e.g. CPU cores), no hardware related third-party IPR licensing issues or royalties
- Minimal size (compared to DSP based base band solutions)
  - Flexible, arbitrary data bit-widths (minimized logic)
  - Enables clock/power vs. chip area trade-offs
  - Inherent parallelism, scales easily (e.g. for 2-arm diversity receiver)
- Available in different configuration and with different interface options, including interface option for I2C or for industry standard AMBA bus.

2 Architecture

2.1 Overview

The basic architecture of a single armed DRM receiver is shown in Fig. 1 below, while Fig. 2 gives an overview of the data flow and the processing blocks inside such a DRM receiver:

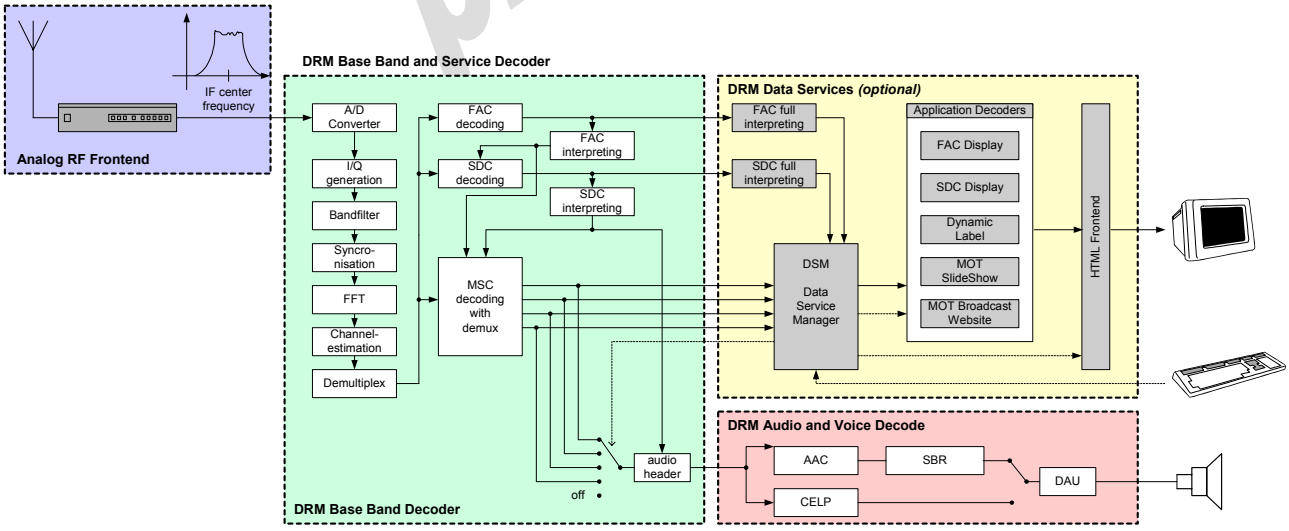

Fig. 1: DRM receiver block diagram

- **Analog RF Front End**: AM and FM (optional) tuner, typically build from COTS components, with intermediate frequency at 10.7 MHz or 455 MHz. For DRM, the signal at the intermediate frequency is further downconverted (digitally or with analog mixer) to base band.
- **DRM Base Band Decoder**: The DRM base band processing IP.
- **DRM Audio and Voice Decode**: Software libraries running on an embedded ARM9 core or any other suitable host processor.
- **DRM Data Services**: Decoder for optional DRM data services, e.g. "MOT Slide Show" and "Broadcast Website" or the news service "Journaline". *Please note:* All data services defined in DAB are defined in DRM as well.

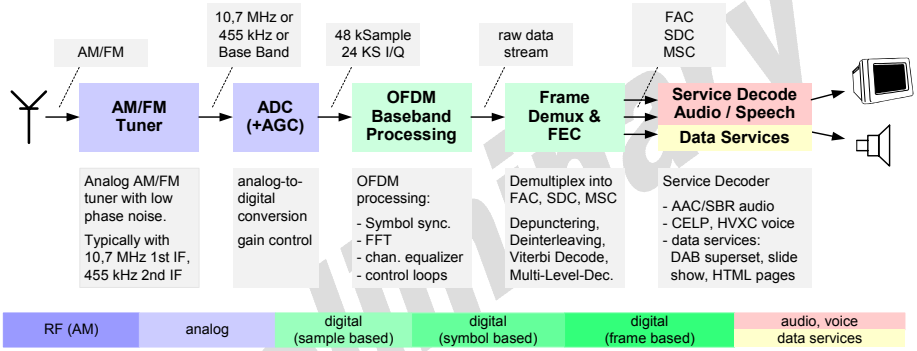

Fig. 2: DRM receiver data flow and processing blocks

2.2 DRM Base Band IP and Interfaces

The CorePool DRM Base Band Decoder IP implements the "OFDM Base Band Processing" and "Frame Demux & FEC" blocks shown in Fig. 2. The DRM Base Band Decoder IP interfaces to the tuner via an ADC (integrated or external) and to the service decoder. This is visualized in Fig. 3 below:

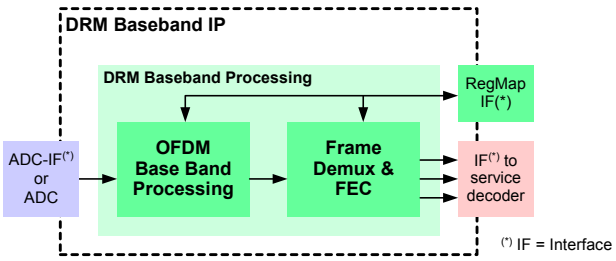

Fig. 3: DRM base band IP

The interfaces to ADC and to the service decoder should be seen as generic interfaces. The DRM Base Band IP supports different interface configurations.

ADC Interface (tuner side)

- **Variant 1** (default) – External analog down conversion to base band, sampling at 48 kbps, using a standard "audio ADC": To connect directly to the integrated or to an external "audio ADC", the industry standard I2S interface is supported.
- **Variant 2** (option) – Direct sampling at 455 kHz IF, with digital down conversion (provided as part of the DRM base band IP). To connect directly to a high speed ADC sampling the 455 kHz IF.
- **Variant 3** (default) – I/Q sample interface, with optional digital down conversion (provided as part of the DRM base band IP). This uses a modified high speed serial version of the I2S interface.

RegMap Interface (DRM "Register Map", Configuration and Control)

This is a bi-directional interface, used to setup, configure and monitor the DRM base band IP. In addition, it allows direct access to most internal memories – simplifying debugging and diagnostics for system integration.

- **Variant 1** (default) – 8-bit bi-directional interface with additional control signals. Allows direct interfacing to most microcontrollers and connection to a PC in a lab setup. Receiver status changes may be monitored (polling) or indicated by additional interrupt signal.
- **Variant 2** (option) – The register map is made available via a standard I2C interface. This is the recommended option for a stand alone (single IC) implementation of the DRM base band IP. The I2C interface will enable normal microcontrollers and processors to configure and control the DRM base band. To indicate receiver status changes, an interrupt output is provided in the DRM base band IP as well.
- **Variant 3** (option) – AMBA Peripheral Bus (APB) Slave Device Interface. This is the recommended option for an integrated implementation. The APB interface will enable other processor cores integrated on the same silicon (SoC) to control the DRM base band. To indicate receiver status changes, an additional interrupt signal is provided by the DRM base band IP.

Service Decoder Interface (DRM Service Multiplex Output)

- **Variant 1** (default) – The DRM Service Multiplex (MDI) is read out via the 8-bit bi-directional interface described in the section "RegMap Interface". This allows direct interfacing to most microcontrollers and connection to a PC in a lab setup.

- **Variant 2** (option) – The DRM Service Multiplex (MDI) is output using a I2S-like serial interface. This is the recommended option for a stand alone (single IC) implementation of the DRM base band IP with service decoding running on an external host processor. The interface outputs "streaming data", a continuous serial data stream with a known maximum bit rate.
- **Variant 3** (option) – The DRM Service Multiplex (MDI) is made available using the AMBA Advance High-performance Bus (AHB) in slave mode. This is the recommended option for an integrated implementation. Data within the DRM service multiplex may be read out by any processor integrated on the same silicon (SoC) and connected to the AHB bus system. Data is provided in packetized (framed) format.

Note: The options described above were used to demonstrate some of the capabilities of the generic interfaces of the DRM base band IP. Not all options are immediately available.

3 DRM Base Band Decoder Specification

3.1 Receiver Capabilities

The CorePool DRM base band receiver IP has been defined in accordance with the DRM standard [1] and in consideration of the minimum receiver requirements currently under discussion in the DRM consortium.

The CorePool DRM base band receiver IP has the properties listed below:

spectrum occupancy	4.5 kHz / 5 kHz 9 kHz / 10 kHz 18 kHz / 20 kHz (option)
robustness modes	A, B, C, D
access to DRM multiplex	decodes and outputs ▪ Fast Access Channel (FAC) ▪ Service Description Channel (SDC) ▪ Main Service Channel (MSC)
DRM multiplex reconfiguration	▪ service reconfiguration: supported (alternative service selection by means of external control processor) ▪ channel reconfiguration: supported
DRM layer	base layer

MSC modes	▪ 64-QAM, non hierarchical ▪ 64-QAM, hierarchical on I ▪ 64-QAM, hierarchical on I&Q ▪ 16-QAM, non hierarchical
SDC modes	▪ 16-QAM ▪ 4-QAM
interleaver depth	400 ms (short interleaver) 2 s (long interleaver)
AFS	supported (dropouts may occur)
services	up to 4 services (audio and/or data), all combinations as defined in [1], section 6
data entities and IDs	data available as received (part of the SDC)
text messages and packet mode	data available as received (part of the SDC)
tuning range and frequency stepping	not applicable (tuner dependent)

4 Appendix

4.1 References

[1] ETSI ES 201 980: "Digital Radio Mondiale (DRM): System Specification", V2.1.1 (2003-10)

[2] ETSI TS 1xx xxx: "Digital Radio Mondiale (DRM): Receiver Status and Control Interface (RSCI)", V0.0.3 (2004-05)

[3] Philips Semiconductors, "The I2C-bus and how to use it (including specifications)", April 1995

[4] ARM, "AMBA™ Specification (Rev 2.0)", 1999